Research Article

Digital Space Vector Approach to Eliminate Overcharging of DC-link Capacitor in Asymmetrical VSI Fed Open End Winding Induction Motor Drive

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Abstract. *Dual inverter topology with asymmetrical input voltage (2:1) is the simple and most economical solution to fabricate four-level output voltage. Due to the lack of switching status selections, the asymmetric configuration of the dual inverter suffers from overload of the DC link capacitor. The present work compares few exiting decoupled and coupled PWM techniques with implementation using multilevel carrier comparison approach and digital space vector approach. It is proved that proposed coupled PWM with the digital space vector approach provide easy path for switching state selection to eliminate the problem "overcharging of DC link capacitor". The other decoupled PWM techniques may eliminate the problem, but generate poor quality of output voltage. In addition, the proposed digital space vector approach provides freedom in the choice of different voltage vectors to achieve good output voltage quality.*

Keywords

Carrier comparison approach,Coupled PWM, Decopuled PWM, Digital space vector approach.

1. Introduction

Medium to high power drives are employed with VSI fed induction motors. PWM techniques are used for voltage and output frequency monitoring [1–3]. The current trend is to use multilevel inverters (MLI) in the blank space of conventional two-level VSI [4–7] to improve the quality of output potential and reduced common mode voltage (CMV). But the conventional topologies of multi-level inverters suffer from major disadvantages such as the problems of balancing capacitors [5] and high power capacitors are necessary to support the charge current. Among the various configurations of multi-level inverters for induction motor drives, open-winding induction motor drives powered by two inverters are increasing in importance [6]. Established along the provision of input DC voltage dual inverter fed open end winding IM drives are classified as symmetrical (1:1 voltage ratio) [7] and asymmetrical (2:1 voltage ratio) dual inverter configurations [8, 9]. Based on the switching scheme used in PWM techniques [10], the asymmetric configuration of the dual inverter (4 levels) generates a higher number of voltage levels relative to the symmetrical configuration of the dual inverter (3 levels). Equally the same circuit configuration is capable of generating higher number of levels, in this article focus is applied to asymmetrical dual inverter configuration.

From the survey it is observed that PWM techniques can be carried out based on carrier compari-

son approach and digital space vector approach [1–3]. In a carrier comparison approach, modulation signals are compared with high-frequency carrier signals for generating control signals. These two-level modulating signals can be generated based on space vector approach [2] and scalar approach [1, 3]. In the digital space vector approach, the instantaneous reference voltage space vector is synthesised by voltage vectors in an average direction by satisfying the volt-sec equilibrium condition. For two-level inverter both these PWM approaches give identical results [2] and many authors, co-related carrier comparison and digital space vector approaches.

In carrier comparison approach for a multilevel inverter (N level inverter), modulating signals are compared to N-1 level shifting carrier signals [11]. In digital space vector approach for multilevel inverters, the actual reference vector shifts to nearest sub hexagon center and nearest voltage vectors are used to synthesize the new reference voltage vector by satisfying the volt second balance condition [11–13].

Two two-level inverters are arranged to form the multilevel inverter configuration (Dual inverter configuration). Hence, based on controlling of two-level inverters, control techniques are classified as coupled PWM techniques [14–16] and decoupled PWM techniques [17]. These PWM techniques may also be carried out using either a carrier comparison approach or a digital spatial vector approach. Based on the analysis of the literature [14–17], decoupled PWM techniques generate poor output voltage quality for asymmetric drives of open-end induction motors powered by dual inverters. On the other hand, coupled PWM techniques generate good output voltage quality, but have the DC-link capacitor overload issue [14, 15]. Overcharging of DC-link capacitor is treated as the grievous problem in the asymmetrical dual inverter fed open end winding induction motor drive because this contributes to limited range of functioning and hence limited speed control.

In order to overcome the DC link capacitor overload problem, various circuit configurations [22] and different decoupled PWM techniques [23, 25–27] were discussed in the literature. All these methods lead to decrease the quality of output voltage and also require modified circuit configurations which may increase the cost and complexity of operation. In [24, 27], a discontinuous PWM technique (implemented in accordance with the carrier comparison approach) was proposed to eliminate over-charging of the DC link capacitor. The downside of this approach is that the required switching states are not selectable. Hence scope of the PWM technique is limited to extend.

As the existing PWM methods [17–29] are implemented using carrier comparison approach (using the concept of switching times), freedom in selecting appropriate voltage vectors in four level space vector plane is not possible. Therefore, in this article, a multilevel digital space vector approach is presented for the asymmetrical double inverter open-winding induction motor drive. A new method of implementation and analysis of multilevel digital space vector based coupled PWM techniques were presented. With inherent simplicity in implementation this digital space vector PWM technique can be extended to N-level inverter. Moreover the digital space vector approach is compared to other space vector based carrier comparison approaches. The proposed digital space vector approach offers the freedom to choose different switching states to eliminate the overcharging of the DC link capacitor with good output voltage quality.

2. Asymmetrical dual inverter fed open end winding induction motor drive

The configuration of the dual inverters with asymmetrical input voltage connected to open winding induction motor is illustrated in Fig. 1. A V_{dc} effective input DC voltage is split in the ratio of 2:1 as $2V_{dc}/3$ to inverter-I and $V_{dc}/3$ to inverter-II. When the switch is ON, it is represented with switching state 1 and similarly when the switch is OFF it is represented by Switching state 0. When top switches in inverter-I are turned ON (Switching state 1), inverter-I will generate a pole voltage of $2V_{dc}/3$. When top switches in inverter-I are turned OFF (Switching state 0), inverter-I will generate a pole voltage of 0. Similarly When top switches in inverter-II are turned ON (Switching state 1), inverter-II will generate a pole voltage of $V_{dc}/3$ else 0. Table1 shows the voltage of each inverter pole and the calculated effective voltage of the dual inverter with asymmetric configuration. Based on the effective pole voltage shown in Table 1, the voltage has four levels ($-V_{dc}/3$, 0, $V_{dc}/3$ and $2V_{dc}/3$). As a result, the asymmetric configuration of the dual inverters is referred to as the four-level inverter configuration.

3. PWM Techniques for asymmetrical dual inverter

The asymmetrical dual inverter fed open end winding induction motor drive is equipped with 2 two-level inverters as shown in Fig. 1. PWM techniques can be applied either by treating the two inverters as one unit or by treating the two inverters as a separate unit. On the basis of this PWM, the dual inverter-powered open-winding induction motor drive techniques are split into

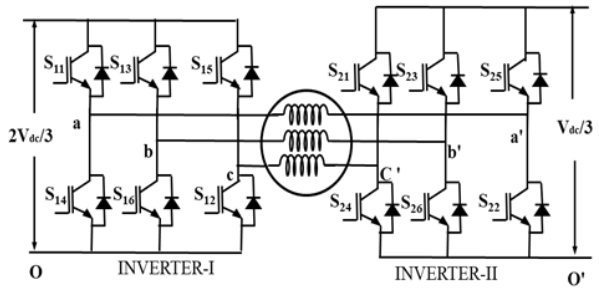

Fig. 1: Drive configuration of the asymmetrical dual inverter with open end winding induction motor.

Tab. 1: Calculation of Phase A Efficient Pole Voltage in dual inverter with Asymmetrical Configuration.

Switching state of S11 in Inverter -I	Inverter -I Pole Voltage	Switching state of S12 in Inverter -II	Inverter -II Pole Voltage	Effective pole Voltage	Switching state of 4-Level SV plane
0	0	1	$V_{dc}/3$	$-V_{dc}/3$	0
0	0	0	0	0	1
1	$2V_{dc}/3$	1	$V_{dc}/3$	$V_{dc}/3$	2
1	$2V_{dc}/3$	0	0	$2V_{dc}/3$	3

two categories as coupled and decoupled PWM techniques.

3.1. Decoupled PWM technique

With a decoupled PWM technique each inverter is treated as a separate unit and command reference signals are independently generated for each two-level inverter by using two-level space vector concept [6] or carrier comparison approach. The space vector plane of teo-level inverter with switching state for inverter-I and inverter-II are shown in Fig. 2(a) and Fig. 2(b). Mathematical formulation of resulting space vector from individual two-level inverters with decoupled space vector PWM is given by (1). Both the methods generate the same pulse pattern. The implementation of the decoupled PWM technique using space vector based

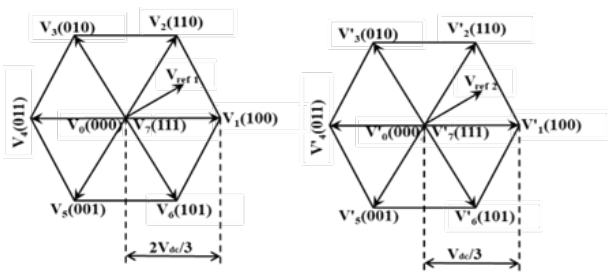

Fig. 2: Space vector plane of (a) Inverter-I (b) inverter-II

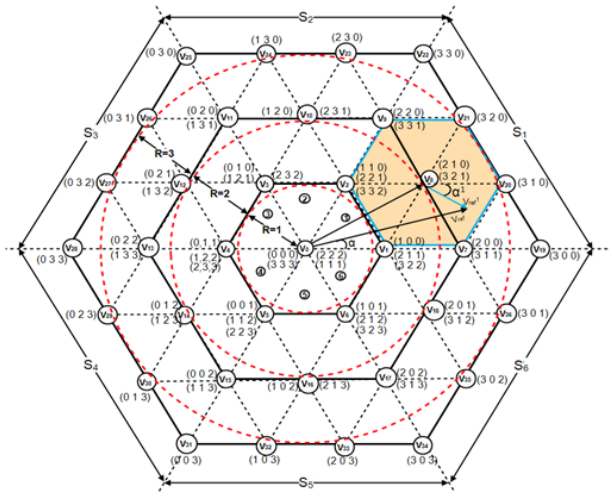

Fig. 3: Space vector plane of a four-level inverter

imaginary switching times is disused in [17–19].

$$\begin{aligned} V_{ref1}\angle\alpha_1 &= V_a + V_b e^{j2\pi/3} + V_c e^{j4\pi/3}, \\ V_{ref2}\angle\alpha_2 &= V_{a'} + V_{b'} e^{j2\pi/3} + V_{c'} e^{j4\pi/3}, \\ V_{ref}\angle\alpha &= V_{ref1}\angle\alpha_1 - V_{ref2}\angle\alpha_2. \end{aligned} \tag{1}$$

where $V_i = V_m \cos(\omega t - 2(r-1)\pi/3)$, $i = a, b, c$, and $r = 1, 2, 3$, $V_{i'} = V_m \cos(\omega t - 2(r-1)\pi/3 - \pi)$.

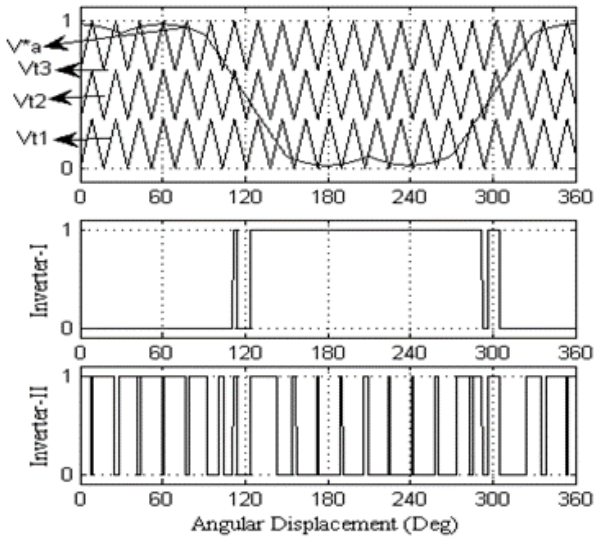

Fig. 4: Realization of carrier comparison approach for control signal generation.

To get maximum output voltage the reference signals or modulating signals for inverter-I (V_a, V_b, V_c) and inverter-II ($V_{a'}$, $V_{b'}$, $V_{c'}$) are considered with a phase shift of 1800 as in (1). In the equivalent space vector approach inverter-I will operate in the first sector and inverter-II will operate in fourth sector. The switching sequence for each inverter in various sectors is given in Table 2 [17].

Tab. 2: Switching sequence of 2-level space vector plane

Sector	Switching states
1	8127-7218
2	8327-7238
3	8347-7438
4	8547-7458
5	8567-7658
6	8167-7618

3.2. Coupled PWM technique

In the coupled PWM technique, the two inverters are treated as one unit (from which the configuration becomes a multilevel inverter configuration). The command, control signals are generated utilizing a tiered digital space vector PWM approach or a tiered carrier comparison approach. The mathematical expression for four-level space vector of asymmetrical dual inverter is given by (2). The four-level space vector plane with switching states is given in Fig. 3. The correlation between switching states of four-level space vector plane with switching states of inverter-I and inverter-II is given in Table 1. The process of selection of switching sates is elaborately discussed in section 4. .

$$V_{ref}\angle\alpha = (V_a - V_{a'}) + (V_b - V_{b'})e^{j2\pi/3} + (V_c - V_{c'})e^{j4\pi/3}$$

$$\begin{aligned} V_{ref}\angle\alpha = &\left(S_{11}\frac{2V_{dc}}{3} - S21\frac{V_{dc}}{3}\right) \\ &+ \left(S13\frac{2V_{dc}}{3} - S23\frac{V_{dc}}{3}\right)e^{j2\pi/3} \\ &+ \left(S15\frac{2V_{dc}}{3} - S25\frac{V_{dc}}{3}\right)e^{j4\pi/3}. \end{aligned} \tag{2}$$

In the four-level space vector plance it is observed that, there is only one switching state for the voltage vectors in the outer most peripheries. For the remaining voltage vectors which are in the innermost periphery there are more than one switching states. The selection among multiple switching states for a single voltage vector yields different PWM techniques. With the selection of few switching states space vector and carrier comparison approaches may or may not give identical pulse pattern.

To obtain equivalent pulse pattern in carrier comparison approach has to be realized with many complex calculations and iterations. Moreover, with the change in modulation index these calculations and iterations changes. Hence, much freedom in selecting optimal switching state with generalized and easier implementation approach is only possible with the multilevel digital space vector approach. This method can be easily extended to any N-level inverter configurations.

The realization of multilevel carrier comparison approach is shown in Fig. 4. Where a two-level basic modulating signal is compared to (three) level shifting carrier signals. The switching logic for generating the control signals is indicated in Table 3 [20].

Tab. 3: Generation of switching logic

Condition	Switch Status
$V_r* > V_{t1}$, $V_r* > V_{t2}$ and $V_r* > V_{t3}$	S_{11}: OFF, S_{14}: ON, S_{21}:ON, S_{24}:OFF
$V_r* > V_{t1}$, $V_r* > V_{t2}$ and $V_r* < V_{t3}$	S_{11}: OFF, S_{14}: ON, S_{21}:OFF, S_{24}:ON
$V_r* > V_{t1}$, $V_r* < V_{t2}$ and $V_r* < V_{t3}$	S_{11}: ON, S_{14}: OFF, S_{21}:ON, S_{24}:OFF
$V_r* < V_{t1}$, $V_r* < V_{t2}$ and $V_r* < V_{t3}$	S_{11}: ON, S_{14}: OFF, S_{21}:OFF, S_{24}:ON

4. Implementation of coupled PWM techniques using digital space vector approach

In this approach the control signals to both the inverters are synthesized treating asymmetrical dual inverters as a single unit. Once the switching states shown in Fig. 3 are synthesized, they are bifurcated using a simple logic given in Table 1. Four-level space plane consists of 64 switching states, each corresponding to different voltage vectors. The space plane may be divided into three regions based on the modulation index. Modulation index (M_i) for an N-level inverter is defined through (3). Where V_dc is the normalized DC-link voltage of a four level inverter. The normalized M_i, M_{in} becomes same as the magnitude of the reference vector, when normalized to $\frac{2}{3}V_{dc}$. V_{ref} takes a maximum value of $\frac{2}{3}V_{dc}\cos 30^o$. The reference vector is assumed to be in the linear modulation range if M_{in} lies in the range of 0 to 2.598. This modulation range, R is further divided into three regions, if $0 < M \leqslant 0.866$, R takes a value 2, if $0.866 < M \leqslant 1.732$, R takes a value 3 and if $1.732 < M \leqslant 2.598$, R takes a value 4. The value of R indirectly specifies the inverter level to synthesize reference voltage. For R=2 the switching states generating two-level output voltage pulse pattern is obtained. Similarly for R=3 and R=4, three-level and four-level pulse pattern is obtained.

$$M_i = \frac{V_{ref}}{\frac{2}{3}V_{dc}}.(n-1), \tag{3a}$$

$$M_{in} = V_{ref}.(n-1). \tag{3b}$$

In any digital space vector approach selection of switching states is achieved by spotting out the triangle in which the tip of V_{ref} lies is to be identified. To constitute the V_{ref} any of the switching states can be selected. But to reduce the ripple nearest switching states should be selected for synthesizing the reference

vector. By clear examination at Fig. 3 it can be observed that the four-level space plane consists of 19 sub hexagons with six triangles per sub hexagon. One such sub hexagon with blue color boundary is indicated in Fig. 3. To find the triangle in which tip of reference vector lies, it is very much essential to identify the sub hexagon in which V_{ref} resides. For easy understanding the reference vector is assumed to be situated in sub hexagon with V_8 as centre making an angle α with reference d-axis. The procedure and formulae involved to synthesize V_{ref} at a given switching instant is explained in the following steps.

Step 1: using the polar from of reference vector $|V_{ref}|\angle\alpha$, sector number and modulation range are identified using (4), (5).

$$S = 1 + fix[\frac{\alpha}{\pi/3}], \tag{4}$$

$$R = 1 + floor[\frac{|V_{ref}|}{0.866}]. \tag{5}$$

Tab. 4: Lookup table of input voltage vectors for generation of NSS

Sector no.	Input Vectors (IV_1, IV_2)
1	$IV_1 = (100), IV_2 = (110)$
2	$IV_1 = (110), IV_2 = (010)$
3	$IV_1 = (010), IV_2 = (011)$
4	$IV_1 = (011), IV_2 = (001)$
5	$IV_1 = (001), IV_2 = (101)$
6	$IV_1 = (101), IV_2 = (100)$

Tab. 5: Selection of Switching States with Conventional 0127 Sequence in S1

Range (R)	NSS	Triangle (T)	Zero sates	Active	sates	Zero sates
			State '0'	State '1'	State '2'	State '7'
1	V_0	1	222	322	332	333
		1	100	200	210	211
2	V_1	2	100	110	210	211
		6	110	210	211	221
	V_2	1	110	210	220	221
		1	200	300	310	311
	V_7	2	200	210	310	311
		6	210	310	311	321
3	V_8	1	210	310	320	321
		2	210	220	320	321
	V_9	6	220	320	321	331
		1	220	320	330	331

To identify the sub hexagon in which the reference vector resides at a given switching instant the possible centre vector states around which a sub hexagon exists is to be identified. For instance if $R = 3$, V_7,V_8, and V_9 are such possibilities. During transit of reference vector along different sectors these voltage vectors are necessary. These are fed in the form of look-up table given in Table 4.

Step 2: The lookup table to identify the input vectors IV_1 and IV_2 is given in Table 3. From Table 3, identify the input vectors at a given switching instant.

Step 3: Given sector number and input vectors IV_1 and IV_2, a matrix, $[SS]_{Rx3}$ containing the probable nearest switching states are synthesized using the following set of equations, given in (6).

$$X = (R-1) * IV_1$$
$$\overset{R}{_{p=1}}SS_p = X - (p-1) * \Delta. \tag{6}$$

where $\Delta = (IV_1 \sim IV_2)$

Step 4: Distance matrix, d_{Rx1} with distance from each switching state to the reference vector state as elements is synthesized using (7).

$$\overset{R}{_{p=1}}d_p = |V_{ref} - SS_p|. \tag{7}$$

Step 5: Identify the nearest switching state (NSS) which is at a minimum distance from the reference vector. This becomes the centre of the sub hexagon in which the tip of reference vector is lying at a given instant.

Step 6: The reference vector is shifted to the sub hexagon with NSS as centre, the d-q axis components of shifted reference vector are obtained using (8).

$$V'_{ref,d} = V_{ref,d} - NSS_d,$$
$$V'_{ref,q} = V_{ref,q} - NSS_q. \tag{8}$$

Here $V'_{ref,d}$, $V_{ref,d}$, NSS_d and $V'_{ref,q}$, $V_{ref,q}$, NSS_q are the d-q axes components of shifted reference vector, original reference vector and NSS respectively. Now the shifted reference vector is given by (9).

$$V'_{ref} = V'_{ref,d} + jV'_{ref,q} \tag{9}$$

Step 7: From the d-q axis components the triangle T in which the shifted reference vector is lying at a given instant is found using (α')

$$\alpha' = \tan^{-1}(\frac{V'_{ref,q}}{V'_{ref,d}}),$$
$$T = 1 + fix[\frac{\alpha'}{\pi/3}]. \tag{10}$$

Step 8: Knowing the sub hexagon and triangle in which the tip of the shifted reference vector lies, the corresponding nearest switching states to synthesize the reference vector are drawn from the look-up table given in Table 5.

Step 9: Once the switching states to be executed are identified, the reference vector V'_{ref} is to be synthesized using the switching states by satisfying the volt-sec balance condition similar to the two-level space vector PWM. The switching states are to be alienated as active switching states and zero switching sates. Based on position of reference vector in different regions (R1

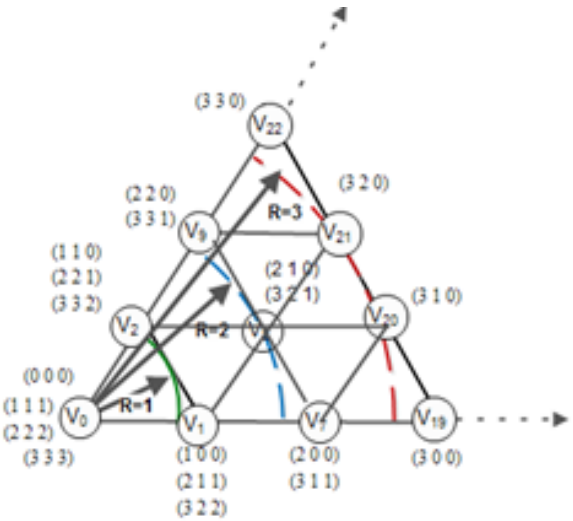

Fig. 5: Zoomed potion of four-level space vector plane in sector S1.

to R3) active vectors and zero vectors are interchangeably used. For simplicity the active sates and zero states in sector S1 shown in Fig. 5 are tabulated in Table 4. As all the sectors (S1-S6) are symmetrical, remaining states can be further tabulated.

Step 10: Knowing the magnitude, position and nearest switching states of the $|V'_{ref}|\angle\alpha'$, the active state and zero state switching times for executing a given sequence is calculated in an average sense. The resulting active vector times and zero vector times are given 11. Here T_a, T_b and T_z are the active state vector and zero state vector dwell times in a given triangle.

$$T_a = |V'_{ref}| * T_s * \left(\frac{\sin(pi/3 - \alpha')}{\sin(\pi/3)}\right), \tag{11a}$$

$$T_b = |V'_{ref}| * T_s * \left(\frac{\sin(\alpha')}{\sin(\pi/3)}\right), \tag{11b}$$

$$T_z = T_s - T_a - T_b, \tag{11c}$$

$$T_7 = 0.5T_z, T_{70} = 0.5T_z. \tag{11d}$$

Step 11: Now the basic PWM technique can be implemented by selecting the switching sates in one switching cycle as in the first column of Table 5. Here in a given switching cycle first zero state is selected flowed by two active states and zero state. As the zero sates are sleeted at the starting and ending of the switching cycle, the zero state time is divide into two equal half's as in 11(d). For this type of switching state in a switching cycle the PWM technique is named as sequence 0127.

Furthermore the approach can be extended to other PWM sequences like bus-clamping (012, 721) involving only one zero state, double-switching bus-clamping sequences involving one zero state and division of either of the active states (0121or 1012, 7212 or 2721). For

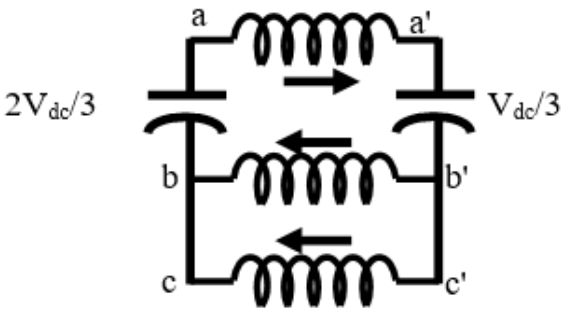

Fig. 6: Equivalent OEWIM drive circuit powered by dual inverter when both inverters are switched with the same impulse model.

Tab. 6: Selection of Switching States with Conventional 0127 Sequence in S1

NSS	R	T	Sequence		
			0127	012	7212
		1	100-200-	100-200-	110-210-
V_1			210-110	210	200-210
		2	110-110-	110-110-	200-210-
	2		210-200	210	110-210
		6	110-210-	110-210-	221-211-
V_2			211-221	211	210-211
		1	110-210-	110-210-	221-220-
			220-221	220	210-220

simplicity the execution of different sequences with reference vector centering at NSS as V_1, V_2 and transiting through different triangles in range 2 is depicted in Table 6. For simplicity the conventional 0127 sequence is considered in this paper. A similar approach can be extended to any PWM sequence with a constraint that it has to maintain volt-second balance in every switching cycle.

5. Analysis of over- charging with different PWM techniques

The asymmetrical configuration of the dual inverter suffers from a major limitation i.e. overcharging of DC link capacitor [20]. This occurs when switching of two inverters happens with same switching states. The equivalent circuit so formed during this switching cycle is shown in Fig. 6. In [20] overcharging of DC link capacitors during various switching cycles is addressed for pulse generation through the traditional carrier comparison approach. In the switching duration where both inverters are conducting the two DC link capacitors C_1 and C_2 come in parallel with respect to ab and a'b' respectively. This causes the C_2 to overcharge at a voltage greater than $V_{dc}/3$ up to $2V_{dc}/3$. This in turn interrupts the maintenance of DC link voltages in the ratio of 2:1. Since the pulse

pattern adapted for the asymmetrical topology is different with the symmetrical topology [20], in this mode of operation it behaves as if asymmetrical pulse pattern is applied to symmetrical topology. The RMS output voltage becomes zero with this operation.

To mitigate this problem some redundant switching states are to be eliminated. From Table 1 and Fig. 3 it is observed that switching states 211, 221, 121, 122, 112 and 212 will generate same pulse pattern to both the inverters. When these switching states are applied the equivalent circuit will be similar to Fig. 6 with sequential change in phase windings connected to C_1 and C_2. From Fig. 3 it is observed that these switching states are positioned at the six corners of a center most hexagon. With the elimination of these switching states overcharging can be eliminated.

5.1. Digital coupled space vector PWM

In the proposed digital approach, as discussed in Section 4. , the realization of inverter output is decided by the magnitude and position of the reference input (Vr). The nearest switching states are selected to reduce the output ripple. When the reference voltage lies in regions R1 and R2 the over-charging, switching states may become the closest states. As a result, C2 gets overcharged. When the reference vector lies in region R3 over-charging switching states will not be the nearest switching states. Consequently, overcharging of the C2 is not observed in R3

In Fig. 3 it is observed that there are three redundant states available at the vertices of the inner most hexagon that can synthesize same output voltage. Among the available three redundant states one state is selected based on the criteria "single switch transition at a time". The resulting switching states in sector S1 after satisfying the conditions is given in Table 5. It is observed that over-charging switching state is selected from three switching states. To eliminate those over-charging switching states in the proposed multilevel digital space vector approach “one switch transition at a time” conditions is not considered. The switching states used for 0127 sequence after eliminating over-charging switching states are given in Table 7. The replaced switching states are highlighted bold (red in color) in Table 7. As the over-charging switching states are eliminated from the total possible switching states, DC-link capacity is maintained as 2:1. The only disadvantage with the elimination of over-charging switching states is that switching losses may slightly increase as the criteria "one switch transition at a time" is not satisfied.

Tab. 7: Selection of Switching States with Conventional 0127 Sequence in S1 for the Elimination of Over-Charging

Range (R)	NSS	Triangle (T)	Zero sates	Active	sates	Zero sates
			State ’0’	State ’1’	State ’2’	State ’7’
1	V_0	1	222	322	332	333
		1	100	200	210	**322**
2	V_1	2	100	110	210	**322**
		6	110	210	**322**	**322**
	V_2	1	110	210	220	**322**
		1	200	300	310	311
	V_7	2	200	210	310	311
		6	210	310	311	321
3	V_8	1	210	310	320	321
		2	210	220	320	321
	V_9	6	220	320	321	331
		1	220	320	330	331

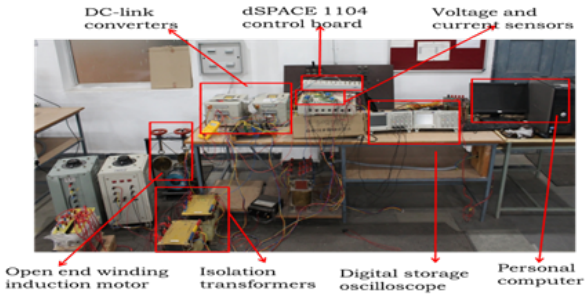

Fig. 7: Prototype model of dual inverter fed open end winding induction motor drive

5.2. Digital decoupled space vector PWM

As disused in section 3. a phase difference of 1800 is considered among the input voltage vector of the first inverter (V_{ref1}) and second inverter (V_{ref2}). If the phase shift is ignored both the inverters will operate with same switching states. (i.e reference vector lies in sector 1 then the switching states would be (8127) for inverter-I and (8’ 1’ 2’ 7’) for inverter-II). When both inverters are operated by same switching states equivalent circuit similar to that of the circuit shown in Fig. 6 will be formed. Hence over-charging of DC-link capacitor is observed with 00 phase shift among the reference voltage vectors.

Among different phase shifts, a phase shift of 1800 is considered to get maximum output voltage. With the phase shift of 1800 the switching states would be (8127) for inverter-I and (8’ 4’ 5’ 7’) would be for inverter-II. With such a switching combination overcharging is eliminated, but the switching states may generate high magnitude of voltage steps [17–19]. This may lead to poor quality of output voltage and high total harmonic distortion. Hence digital decoupled PWM with phase shift of 1800 will eliminate overcharging of capacitors, but results output voltage with high harmonic content when compared to digital coupled space vector PWM.

5.3. Two-level modulating signal based carrier comparison approach

With two-level modulating signal based carrier comparison approach the selection of all of all possible switching states is not possible. With the realization of control signals using the modulating signal shown in Fig. 4 possibility of charging of capacitors beyond their capacity may takes place [20]. This can be addressed with discontinuous modulating signal based PWM techniques and is considered in the literature [20]. The disadvantage of this approach is required switching states cannot be selected. Hence scope of the PWM technique is limited to extend.

6. Results and Discussion

The hypothetical analysis of various PWM techniques fed to the proposed induction motor drive with open end terminals by two inverters feeding the drive is carried in MATLAB. The algebraic expression of phase voltages expressed in terms of pole voltages are shown in (12). The zero sequence voltage for the said drive using (12) is formulated in (13). The phase voltages and zero sequence voltage for different switching states in sector S1 is given in Table 8. Similarly, it can be calculated for remaining switching states using (12) and (13).

$$\begin{aligned} V_{aa'} &= \frac{2}{3}V_{aoa'o'} - \frac{1}{3}V_{bob'o'} - \frac{1}{3}V_{coc'o'}, \\ V_{bb'} &= \frac{2}{3}V_{bob'o'} - \frac{1}{3}V_{aoa'o'} - \frac{1}{3}V_{coc'o',}, \\ V_{cc'} &= \frac{2}{3}V_{coc'o'} - \frac{1}{3}V_{bob'o'} - \frac{1}{3}V_{aoa'o'}. \end{aligned} \tag{12}$$

$$\begin{aligned} V_{ZSV} &= V_{ZSV1} - V_{ZSV2}, \\ V_{OO'} &= \frac{V_{ao} - V_{a'o'} + V_{bo} - V_{b'o'} + V_{co} - V_{c'o'}}{3}, \\ &= \frac{V_{aoa'o'} + V_{bob'o'} + V_{coc'o'}}{3}. \end{aligned} \tag{13}$$

To validate the hypothetical analysis a prototype model of the drive is developed. The built in prototype model is shown in Fig. 7. In the prototype mode DC-link inverters of 9.2 kVA are connected to 415V, 50Hz and 10A rated drive. The DC link converter uses a SKYPER 32R driver IC to provide a dead time of 4.3µsec. This dead time had kept constant for all present PWM techniques. The PWM signals for DC-link dual inverters are synthesized using control board, dSPACE 1104. The switching frequency of the pulse signals is fixed at 1 kHz. A DC voltage of 510V is shared among the inverters in 2:1 ratio of to both the inverters. To capture the results a voltage regulator

Tab. 8: Calculation of Phase A Efficient Pole Voltage in dual inverter with Asymmetrical Configuration.

Switching states	Effective phase voltage	Zero sequence voltage	Switching states voltage	Effective phase	Zero sequence voltage
000	0	$-V_{dc}/3$	200	$4V_{dc}/9$	$-V_{dc}/9$
111	0	0	311	$4V_{dc}/9$	$2V_{dc}/9$
222	0	$V_{dc}/3$	321	$3V_{dc}/9$	$3V_{dc}/9$
333	0	$2V_{dc}/3$	210	$3V_{dc}/9$	0
100	$2V_{dc}/9$	$-2V_{dc}/9$	331	$V_{dc}/9$	$4V_{dc}/9$
211	$2V_{dc}/9$	$V_{dc}/9$	220	$V_{dc}/9$	Vdc/9
322	$2V_{dc}/9$	$4V_{dc}/9$	300	$6V_{dc}/9$	0
332	$V_{dc}/9$	$5V_{dc}/9$	310	$5V_{dc}/9$	$V_{dc}/9$
221	$V_{dc}/9$	$2V_{dc}/9$	320	$4V_{dc}/9$	$2V_{dc}/9$
110	$V_{dc}/9$	$-V_{dc}/9$	330	$V_{dc}/9$	$3V_{dc}/9$

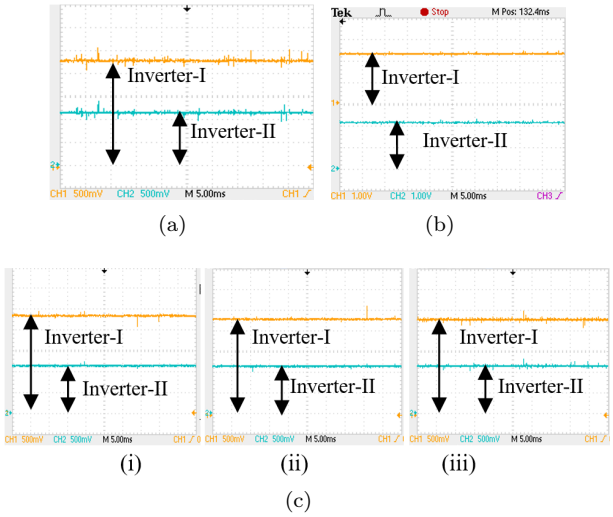

Fig. 8: DC-link capacitor voltages of inverter-I and Inverter-II with different PWM techniques (a) Digital Decoupled space vector PWM (M=0.52) (b) Two-level modulating signal based carrier comparison approach (M=0.52) (c) Digital coupled space vector PWM (at M=0.67, M=1.56, M=2.49).

LV20-P (500 V to 3.3 V) and current sensor (50A to 3.3 V with one turn) LA-55P are used.

The DC-link voltages of two inverters with various PWM techniques are shown in Fig. 8 at varied modulation values. The captured results from 1 MHz Tetronix DSO are made available in Fig. 8 and are compatible with the simulation study and the concept discussed in section 5. .

The DC-link voltages of two inverters with various PWM techniques are shown in Fig. 8 at varied modulation values. The captured results from 1 MHz Tetronix DSO are made available in Fig. 8 and are compatible with the simulation study and the concept discussed in section 5. With decoupled and coupled space vector PWM techniques the overcharging of two capacitors C1 and C2 is controlled in the entire modulation range. To validate the test results the capacitor voltage levels

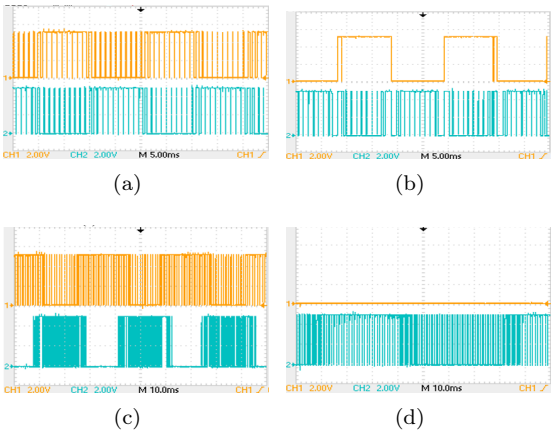

Fig. 9: Pulse pattern for inverter-I and inverter-I with different PWM techniques (a) Digital decoupled space vector based PWM technique at M=0.83 (b) Digital coupled space vector based PWM technique at M=2.49 (c) Digital coupled space vector based PWM technique at M=1.56 (d) Digital coupled space vector based PWM technique at M=0.67.

are shown in Fig. 8(a) and Fig. 8(c) and are maintained at 2:1 ratio. There is a substantial amount of improvement when compared with two-level modulating signal based carrier comparison approach. This is because in that method only for a limited modulation range, greater than 0.9 the overcharging of capacitors is avoided. But for the remaining range it is seen prominently [20]. Fig. 8(b) depicts that the DC link voltage of C2 has overcharged to the voltage equal to that of C1 resulting in violating the principle asymmetrical dual inverter operation of maintaining 2:1 ratio.

The experimental results of pulse pattern to inverters, various voltages and currents of the drive fed with two inverters integrated with digital space vector based PWM technique at different modulation index are shown in Fig. 9 and Fig. 10. From the pulse pattern of digital decoupled space vector PWM shown in Fig. 9(a), it is concluded that both inverters are continuously switched at all the modulation indices. Because of this continuous switching pattern the six corner voltage vectors of outer most hexagon (V19, V25...) and center most voltage vectors (V0) will be selected or used to constitute effective voltage of dual inverter. Because of the selection of non nearest voltage vector of three-level space vector plane these are a high error voltage between instantaneous applied voltage vector and reference voltage vector. Hence the high magnitude of voltage levels will be created in the voltage plots. With digital decoupled space vector PWM the effective phase voltage plot shown in Fig. 10(a),(i) is having a voltage step of magnitudes $6V_{dc}/9$, $4V_{dc}/9$, $2V_{dc}/9$ and $V_{dc}/9$ at all the modulation indices. The obtained voltage levels or steps in the effective phase voltage plot are same as the theoretical calculations given in Table 8.

From the pulse pattern of digital coupled space vector PWM shown in Fig. 9 (9(b), 9(c), 9(d)), it is observed that both inverters are not continuously switched. Moreover, it is also observed from the analysis that all the possible nearest voltage vectors are used to constitute effective voltage of dual inverter. Hence the magnitude of the error voltage vector is less and this lead to low magnitude of voltage step. With digital coupled space vector PWM is shown in Fig. 10(b), (i) effective phase voltage is having a voltage step with magnitudes $2V_{dc}/9$ and $V_{dc}/9$ at all the modulation indices. Hence, with both the digital PWM techniques numbers of voltage levels or steps are same, but the magnitudes of voltage steps are different. With a high magnitude of voltage steps $5V_{dc}/9$, $4V_{dc}/9$ total harmonic distortion (THD) is high with digital decoupled space vector PWM when compared to digital coupled space vector PWM.

The same can be observed from THD plots shown in Fig. 10. From, Fig. 10 (10(c), 10(d)) it is observed that with the change in modulation indices magnitude of voltage step remains same but number of voltage steps are changing with coupled space vector PWM. But with decoupled space vector PWM magnitude of voltage step and number of voltage levels remains same only change will be there in the pulse width [17–19].With digital coupled space vector PWM technique as the modulation index increases voltage THD decreases as observed in Fig. 10(iii) (10(b), 10(c), 10(d)). As voltage harmonics are decreasing current harmonics will also decrease, hence the THD plot shown in Fig. 10(iv) (10(b), 10(c), 10(d)) decreases with increase in modulation index.

The calculated zero sequence voltage (ZSV) level for different switching states are given in Table 8. In the proposed digital decoupled PWM technique to eliminate overcharging effect, switching states (211, 221, 121, 122, 112 and 212) are replaced by (322, 332,...). Because of this the magnitude of ZSV is increased from $V_{dc}/9$ to $4V_{dc}/9$ or $2V_{dc}/9$ to $5V_{dc}/9$. Hence an increase in magnitude of $3V_{dc}/9$ is observed, which may lead to increased stress on isolation transformer. The plots of zero sequence voltage with digital coupled space vector PWM shown in Fig. 10(ii) (10(b), 10(c), 10(d)) at various modulation indices. From the theoretical analysis and experimental results it is observed that in the region R2 the ZSV is high. This is because of non selection of overcharging voltage vectors. The plots of ZSV with digital decoupled space vector PWM is shown in Fig. 10(a)(ii). Because of selection of corner most voltage vectors of the outer most hexagon, the ZSV is having a voltage step of 0, $V_{dc}/9$, $2V_{dc}/9$ and $3V_{dc}/9$ constituting a peak to peak magnitude of $V_{dc}/3$ over the entire modulation range.

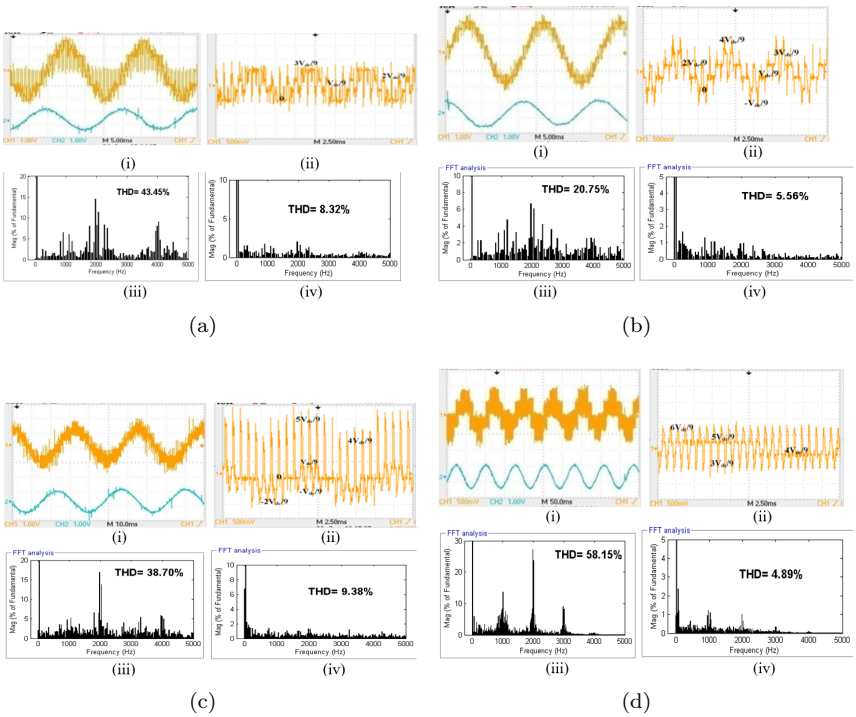

Fig. 10: (i) Effective phase voltage and phase current (ii) Zero sequence voltage (iii) Effective phase voltage THD (iv) phase current THD with (a) Digital decoupled space vector based PWM technique at M=0.83 (b) Digital coupled space vector based PWM technique at M=2.49 (c) Digital coupled space vector based PWM technique at M=1.56 (d) Digital coupled space vector based PWM technique at M=0.67.

7. Conclusion

This paper mainly focuses on eliminating overcharging of DC link capacity, with better quality of output voltage. From the analysis of switching states it is observed that by elimination of switching states 211, 221, 121, 122, 112 and 212 overcharging of DC link capacitors is eliminate. With the remaining switching states it is possible to maintain desired asymmetrical voltage ration and hence the drive can be operated over a wide range of speed, maintaining fine quality of output voltage. From the results it is observed that coupled PWM technique has improved the quality of output voltage when compared to decoupled PWM techniques.

References

[1] Hava, A.M., R.J Kerkmam and T.A Lipo. Simple analytical and graphical methods for carrier based PWM VSI drives. *IEEE Trans. Power Electronics.* 1999, vol. 14, no. 1, pp. 49-61. DOI: 10.1109/63.737592.

[2] Narayanan, G. and V. T. Ranganathan. Triangle comparison and space vector approaches to pulse width modulation in inverter-fed drives. *J. Indian Inst. Sci.* 2000, vol. 80, pp. 409–427.

[3] Silva, E. R. C D., E. C. D. Santos, and C. B. Jacobina. Pulse Width Modulation Strategies. *IEEE ind. Electron. Mag.* 2011, vol. 5, pp. 31-45. DOI: 10.1109/MIE.2011.941120.

[4] Rodríguez, J., J.-S. Lai. Multilevel Inverters: A Survey of Topologies, Controls and Applications. *IEEE Trans. Ind. Elec.* 2002, vol. 49, iss. 4, pp. 724-737. DOI: 10.1109/TIE.2002.801052.

[5] Adam, G. P., S. J. Finney, A. M. Massoud, and B. W. Williams. Capacitor Balance Issues of the Diode-Clamped Multilevel Inverter Operated in a Quasi Two-State Mode. *IEEE Trans. Ind. Electron.* 2008, vol. 55, iss. 8, pp. 3088 - 3099. DOI: 10.1109/TIE.2008.922607.

[6] Stemmler, H., and Guggenbach, P. Configurations of high-power voltage-source inverter drives. In: *Proc. EPE Conf.*, Brighton, UK : IEEE, 1993, pp .7–14.

[7] Shivakumar, E. G., K Gopakumar, S.K. Sinha, AndrePittet, V.T Ranganathan. Space vector PWM for dual inverter fed open-end winding induction drive. *APEC 2001. Sixteenth Annual IEEE Applied Power Electronics Conference and Exposition (Cat. No.01CH37181).* Anaheim, CA, USA: IEEE, 2001, pp. 399-405. DOI: 10.1109/APEC.2001.911678.

[8] Somasekhar, V. T., K. Gopakumar, E. G. Shivakumar, and A. Pittet. Multilevel voltage space vector generation for an open-end winding induction motor drive using a dual-inverter scheme with asymmetrical D.C.—Link voltages. *EPE Journal*. 2002, vol. 12, iss. 3, pp. 21–29. DOI: 10.1080/09398368.2002.11463508.

[9] Reddy, B. V., V. T. Somasekhar, and Y. Kalyan. A Dual Inverter fed four level open-end winding induction motor drive with a nested Rectifier –Inverter. *IEEE Trans. Ind. Informatics*. 2013, vol. 9, iss. 2, pp. 938–946. DOI: 10.1109/TII.2012.2223224.

[10] Grath, B.P Mc and D.G Holmes. Multicarrier PWM strategies for multilevel invertir. *IEEE Trans. Ind. Electron.* 2002, vol. 49, iss. 4, pp. 858-867. DOI: 10.1109/TIE.2002.801073.

[11] Baneerjee, D., R. Ghosh, G.Narayanan and V.T Ranganathan. Comparison of various sine-triangle PWM techniques for three level voltage source inverters in space vector domain. In: *proc. NPEC IIT Kharagpur*. West Bengal, India : IEEE, 2005, pp. 2482-2488. DOI: 10.1109/IAS.2000.883171.

[12] Yao, W. X., H. B. Hu and Z. Y. Lu. Comparison of carrier based modulation and space vector modulation of multilevel inverters. *IEEE Trans. Power electron.* 2008, vol. 23, iss. 1, pp. 45-51. DOI: 10.1109/TPEL.2007.911865.

[13] pereiar, I. and A.Martins. Multicarrier and space vector modulation three phase NPC converters. In: *Proc. 13th EPE*, Barceloan, Spain : IEEE, 2009, pp. 2345-2444.

[14] Shivakumar, E. G., V. T. Somasekhar, K. K. Mohapatra, K. Copakumar, L. Umanand, and S. K. Sinha. A multi level space phasor based PWM strategy for an open-end winding induction motor drive using two inverters with different dc link voltages. In *Proc. 4th IEEE Int. Conf. Power-Electron. Drive Syst.* Indonesia: IEEE, 2001, pp. 169–175. DOI: 10.1109/PEDS.2001.975306.

[15] Somasekhar, V. T., K. Gopakumar, E.G. Shivakumar, and A. Pittet. A multilevel voltage space vector generation for an open-end winding induction motor drive using a dual-inverter scheme with asymmetrical d.c.—Link voltages. *EPE Journal*. 2002, vol. 12, iss. 3, pp. 21–29(2002). DOI: 10.1080/09398368.2002.11463508.

[16] Reddy, M. H. V., T. B. Reddy, B. R. Reddy, M. Suryakalavati. Reduction of Common Mode Voltage in Asymmetrical Dual Inverter Configuration Using Discontinuous Modulating Signal Based PWM Technique. *Journal of Power Electronics*. 2015, vol. 15, iss. 6, pp. 1524-1532. DOI: 10.6113/JPE.2015.15.6.1524.

[17] Reddy, B. V., V. T. Somasekhar, and Y. Kalyan.: Decoupled space-vector PWM strategies for a four-level asymmetrical open-end winding induction motor drive with waveform symmetries. *IEEE Trans. Ind. Electron.* 2011, vol. 58, iss. 11, pp. 5130–5141. DOI: 10.1109/TIE.2011.2116759.

[18] Naganathan, P. and S. Srinivas. Voltage-Injected PWM Variants for a Dual Two-Level Inverter-Fed Open-End Winding Induction Motor Drive. *IEEE Journal Of Emerging And Selected Topics In Power Electronics*. 2020, vol. 9, iss. 2, pp. 1532-1540. DOI: 10.1109/JESTPE.2020.2972279

[19] Mohan, L., K. Pant, P. P. Rajeevan. A Speed Range Extension Scheme for Scalar-Controlled Open-End Winding Induction Motor Drives. *IEEE Trans. on Industry Applications*. 2022, vol. 58, iss. 2, pp. 2055-2062. DOI: 10.1109/TIA.2022.3140284.

[20] Amerise, A., M. Mengoni, L. Vancini, G. Rizzoli, L. Zarri, and A. Tani. Over rmodulation Strategies for an Open-End Winding Induction Motor Drive With a Floating Capacitor Bridge. *IEEE Trans. on Industrial Elec.* 2023, vol. 70, iss. 11, pp. 11033-11043. DOI: 10.1109/TIE.2022.3227302.

[21] Surana, P., M. G. Majumder, R. Resalayyan, K. Gopakumar, L. Umanand and W. Jarzyna. A Fault-Tolerant 24-Sided Voltage Space Vector Structure for Open-End Winding Induction Motor Drive. *IEEE Trans. on Power Electronics*. 2022, vol. 37, iss. 9, pp. 10738-10746. DOI: 10.1109/TPEL.2022.3167161.

[22] Reddy, B. V. and V. T. Somasekhar. A dual inverter fed four-level open-end winding induction motor drive with a nested rectifier-inverter. *IEEE Trans. Ind. Informat.* 2013, vol. 9, iss. 2, pp. 938–946. DOI: 10.1109/TII.2012.2223224.

[23] Lakhimsetty, S., N. Surulivel and V. T. Somasekhar. Improvised SVPWM Strategies for an Enhanced Performance for a Four-Level Open-End Winding Induction Motor Drive. *IEEE Trans. Ind. Electron.* 2017, vol. 64, iss. 4, pp. 2750–2759. DOI: 10.1109/TIE.2016.2632059.

[24] Reddy, M. H. V., T. B. Reddy, B. R. Reddy, M. Suryakalavati. Discontinuous PWM Technique for the Asymmetrical Dual Inverter Configuration to Eliminate the Overcharging of DC-link Capacitor. *IEEE Trans. Ind. Electron.* 2018, vol. 65, iss. 1, pp. 156-166. DOI: 10.1109/TIE.2017.2716858.

[25] Rovere, L., A. Formentini, G. L. Calzo, P. Zanchetta and T. Cox. Zero-Sequence Voltage Elimination for Dual-Fed Common DC-Link Open-End Winding PMSM High-Speed Starter–Generator—Part I: Modulation. *IEEE Transactions on Industry Applications*. 2019, vol. 55, iss. 6, pp. 7804 – 7812. DOI: 10.1109/TIA.2019.2907073

[26] Lee, K., Y. Han. Discontinuous PWM Scheme for an Open-end Winding Induction Motor Drives Fed by Dual Inverter. In: *2022 IEEE Energy Conversion Congress and Exposition (ECCE)*. Detroit, MI, USA: IEEE, 2022, pp. 1-6. DOI: 10.1109/ECCE50734.2022.9947437.

[27] Zerdani, M., S. A. E. M. Ardjoun, H. Chafouk, M. Denai. Experimental Investigation of Decoupled Discontinuous PWM Strategies in Open-End Winding Induction Motor Supplied by a Common DC-Link. *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 2023, vol. 11, iss. 3, pp. 3087 - 3096. DOI: 10.1109/JESTPE.2023.3258799.

[28] Safsouf, K., J. Sawma and H. Y. Kanaan. Enhanced Power-Sharing Control Algorithm for Dual-Inverter-Fed Open-End-Winding Induction Motor in Hybrid Electric Vehicles. In: *2023 IEEE International Conference on Industrial Technology (ICIT)*. Orlando, FL, USA: IEEE, 2023, pp. 1-6. DOI: 10.1109/ICIT58465.2023.10143097.

[29] Jain, S., S V S P. K. Ch, V. Sonti, S. Kumar. Multicarrier Space Vector Pulse Width Modulation for Enhanced Performance of Field Oriented Controlled Open End Winding Induction Motor. In: *2023 IEEE 3rd International Conference on Smart Technologies for Power, Energy and Control (STPEC)*. Bhubaneswar, India: IEE, 2023, pp. 1-6. DOI: 10.1109/STPEC59253.2023.10431019.